What is claimed is:

1. A semiconductor device comprising:

a plurality of metal wire patterns, each of which includes a fine line pattern and pad patterns, wherein an area ratio of the fine line pattern to an overall wire pattern is greater than 1%.

2. The semiconductor device as recited in claim 1, wherein a width of the fine line pattern is below sub-micron.

3. The semiconductor device as recited in claim 1, wherein the pad patterns include connection pad patterns which electrically connect the pad patterns to the fine line pattern, said connection pad patterns being included in said overall wire pattern.

4. The semiconductor device as recited in claim 1, wherein the metal wire patterns are made of aluminum or copper.

5. A semiconductor device comprising:

a plurality of metal wire patterns, each of which includes main fine line patterns, main pad patterns and dummy fine line patterns, wherein an area ratio of the dummy fine line patterns, which are connected to the pad patterns, to an entire wire

pattern is less than 1% and lower than that of an area ratio of the main fine line patterns to the entire wire pattern.

6. The semiconductor device as recited in claim 5, wherein the dummy fine line patterns are formed parallel with the main fine line patterns at a distance of a width of the main fine line pattern.

7. The semiconductor device as recited in claim 5, wherein the metal wire patterns are made of aluminum or copper wire.

8. The semiconductor device as recited in claim 5, wherein the dummy fine line patterns do not make any electric circuit.

9. The semiconductor device as recited in claim 5, wherein the metal wire patterns further include dummy pad patterns, to which the dummy fine line patterns are connected, wherein the dummy pad patterns and the dummy fine line patterns are electrically disconnected from the main fine line patterns and the main pad patterns.

10. The semiconductor device as recited in claim 5, wherein the metal wire patterns further include dummy pad pool patterns, to which the dummy fine line patterns are connected, wherein the dummy pad pool patterns and the dummy fine line patterns are

electrically disconnected from the main fine line patterns and the main pad patterns.

11. The semiconductor device as recited in claim 5, wherein the metal wire patterns are made of aluminum or copper wire.